s lection list may be g n rated by a physical violations detector within the floorplanning tool. The physical violations could be due to overlapping cells, off-grid cells, or any other placement related violation. The physical violations detector is further described in U.S. Patent Application Serial No. 08/789,024 (DRA-3426), filed January 27, 1997, entitled "Method and Apparatus for Identifying Physical Errors in a Placement Database".

In addition, the cell selection list may be generated by an external timing tool and/or physical checking tool. As described in U.S. Patent Application Serial No. 08/598,506, filed February 7, 1996 entitled "Method and Apparatus for Performing Drive Strength Adjust Optimization in a Circuit Design", this tool may provide a cell selection list that includes a listing of cells that violate timing, capacitance, length, etc. requirements. The placement tool may then read the cell selection list and sequentially view the cells listed therein.

Further, the cell selection list may be generated by an "add net cells to overlap" feature of the placement tool. This option may build a cell selection list that includes cells that interface with selected nets within the design. That is, the circuit designer may select a number of critical nets, and the placement tool may assemble a cell selection list containing all cells connected to those selected nets. This may be particularly useful, for

floorplan editor 130. The display terminal is used to display the current cell and surrounding cells. In a preferred embodiment, the cell selection/view control block 120 selects the current cell from the cell selection list 114, and zooms in and displays the current cell on the display device. Thereafter, the user may use the floorplan editor 130 via interface 132 to edit the floorplan file to correct the detected physical violation. After each of the cells identified in the cell selection list 114 has been sequentially operated upon by the cell selection/view control block, the user may direct the floorplan editor to store the floorplan file via interface 134. The above design process is also described in U.S. Patent Application Serial No. ~~DRA-3426~~ 08/789,024, filed January 27, 1997, entitled "Method and Apparatus for Identifying Physical Errors in a Placement Database".

The above method is extremely valuable, particularly since large number of errors may be detected by the physical violations checker block 110. In the past, a circuit designer typically had to manually locate each violation by panning through the design in a floorplanning graphics window. Even when the exact location of a violation was known, navigating to that point could be slow, since the graphics terminal was often manipulating files containing tens of thousands of gates.

It is contemplated that the physical violations checker

in a physical window. By sorting the un-placed cells in a predetermined way (e.g. by a corresponding net name or instance name), the circuit designer may more easily find a desired cell or region for placement.

In prior floorplanning tools, and as indicated above, when a context was loaded, all of the children cells appeared as a pseudo random list of names in a physical window. Since large contexts often contain thousands of instance names, the physical window provided little utility during the placement process. The circuit designer simply had to scroll through the often lengthy list of instances in an attempt to identify the desired object. It was often more efficient for the circuit designer to determine an instance name by cross-referencing an external listing so that the name could be entered manually prior to placement.

A further advantage of the net/instance sort block 136 is that a circuit designer may more easily define object groups, thereby allowing user defined group operations to more readily be performed. For example, a circuit designer may place all drivers for a vectored net by first performing a net sort, and then placing the first component in the group and specifying a direction for further group placement. The floorplanning tool may then incorporate features that allow the circuit designer to place all remaining cells in the group automatically (see for example, U.S. Patent Application No. ~~DRA-3423~~ 08/789,028, filed ~~January~~ January 27, 1997

of th cells and indicating a placement directi n and spacing for the remaining cells of the stack. The stack mode control block 142 may automatically place the remaining cells in the specified direction and at the specified spacing. The stack mode control block is more fully described in U.S. Patent Application Serial No. ~~DRA-3423~~ 08/789,028, filed January 27, 1997, entitled "Method and Apparatus for Associating Selected Circuit Instances and for Performing a Group Operation Thereon".

Finally, data processing system 92 may include a vector filter block 144. Vectored filter block 144 may be coupled to the cell selection/view control block 120. Vector filter block 144 may allow a user to view only those vectored nets that are wider than a predetermined threshold, narrower than a predetermined threshold, or fall within a predetermined range. This may reduce the visual complexity of the circuit design on the display device, and may allow the circuit designer to more effectively analyze vectored net paths. A further discussion of the vector filter 144 can be found in U.S. Patent Application Serial No. ~~DRA-3424~~ 08/789,027, filed January 29, 1997, entitled "Method and Apparatus for Selectively Viewing Nets Within a Database Editor Tool".

FI . 10 is a top view of a partially placed integrated circuit die, having a number of physical errors therein. The diagram is generally shown at 530. Region-A is placed as shown at 532. Region-B 534, region-C 540 and region-D 546 are placed within the outer placement boundary 533 of region-A 532. Likewise, region-E 536 and region-F 538 are placed within the outer placement boundary 535 of region-B 535. Similarly, region-E 548 is placed within the outer placement boundary 545 of region-D 546. Finally, region-F 544 is placed within the outer placement boundary 541 of region-C 540.

In accordance with a preferred embodiment of the present invention, the placement tool may include a physical violations checking feature to identify physical violations in the placement database. The physical violations checking feature may assemble a listing of cells that are involved in physical violations and provide that list as a cell selection list.

The physical violation checking feature of a preferred embodiment of the present invention is described in U.S. Patent Application Serial No. ~~DRA-3426~~ 08/789,024, filed January 27, 1997, entitled "Method and Apparatus for Identifying Physical Errors in a Placement Database". Described therein are a number of physical checks that may be provided by a floorplanning tool, including object overlap checks, object out-of-bounds checks, and object out-of-context checks. A

context. That is, the circuit designer may place a lower-level cell outside of the context of the corresponding higher-level object. Thus, in a preferred embodiment, the floorplanning tool may identify all objects that are placed "out-of-context", and may provide a listing of those objects to a cell selection list. In the illustrated embodiment of FIG. 10, the floorplanning tool may identify region-E 542 as being placed "out-of-context", and may list region-E 542 in a cell selection list.

Another approach for out-of-context checking is to check whether a particular cell is moved from the logical context from which it originated. A "context" may be considered a logical hierarchical level in the logical database. The placement database may have a similar hierarchical structure. However, in a preferred floorplanning tool, a cell or region may be moved from its parent in the placement database to another location in the hierarchical structure. When this occurs, the hierarchical structure of the placement database may no longer match the hierarchical structure of the logical database. This moved cell is then called "out-of-context". The out-of-context check may check for this type of situation and may warn the user thereof.

In addition, region-X 550 and region-Y 552 overlap one another. The object overlap check described in U.S. Patent Application Serial No. ~~DRA-3426~~ 08/789,024, filed January 27, 1997,

entitled "Method and Apparatus for Id ntifying Physical Errors in a Placement Database" may identify region-X 550 and region-Y 552 as overlapping cells, and may list region-X 550 and region-Y 552 in the cell selection list.

Finally, region-Z 554 is placed outside of the boundary defining the integrated circuit die. The object out-of-bounds check described in U.S. Patent Application Serial No. 08/789,024 ~~DRA-3426~~, filed January 27, 1997, entitled "Method and Apparatus for Identifying Physical Errors in a Placement Database" may identify region-Z 554 as being placed outside of the boundary defining the integrated circuit die, and may list region-Z 554 in the cell selection list. This illustrates one of several methods of generating a cell selection list in accordance with the present invention.